

Fig. 1

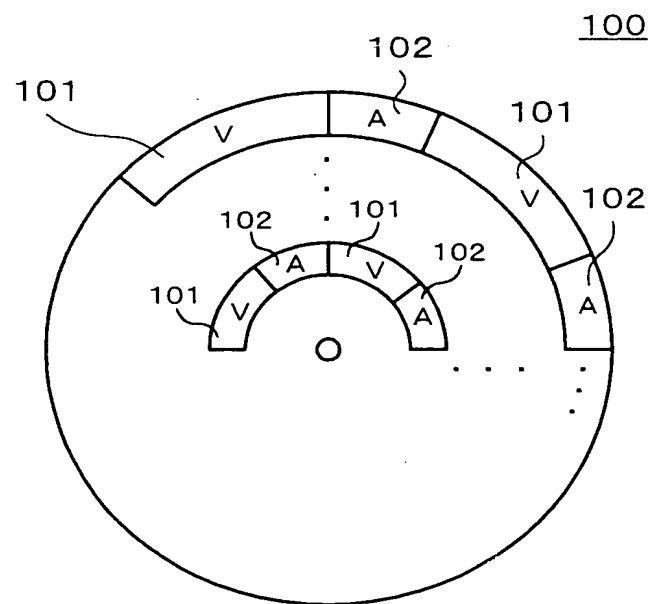


Fig. 2

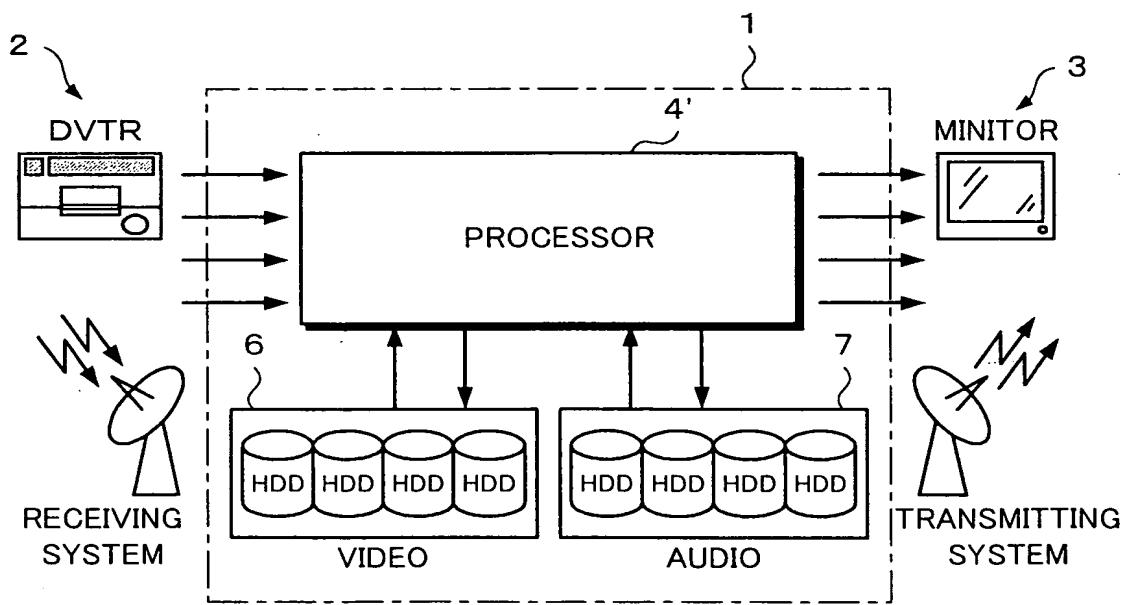
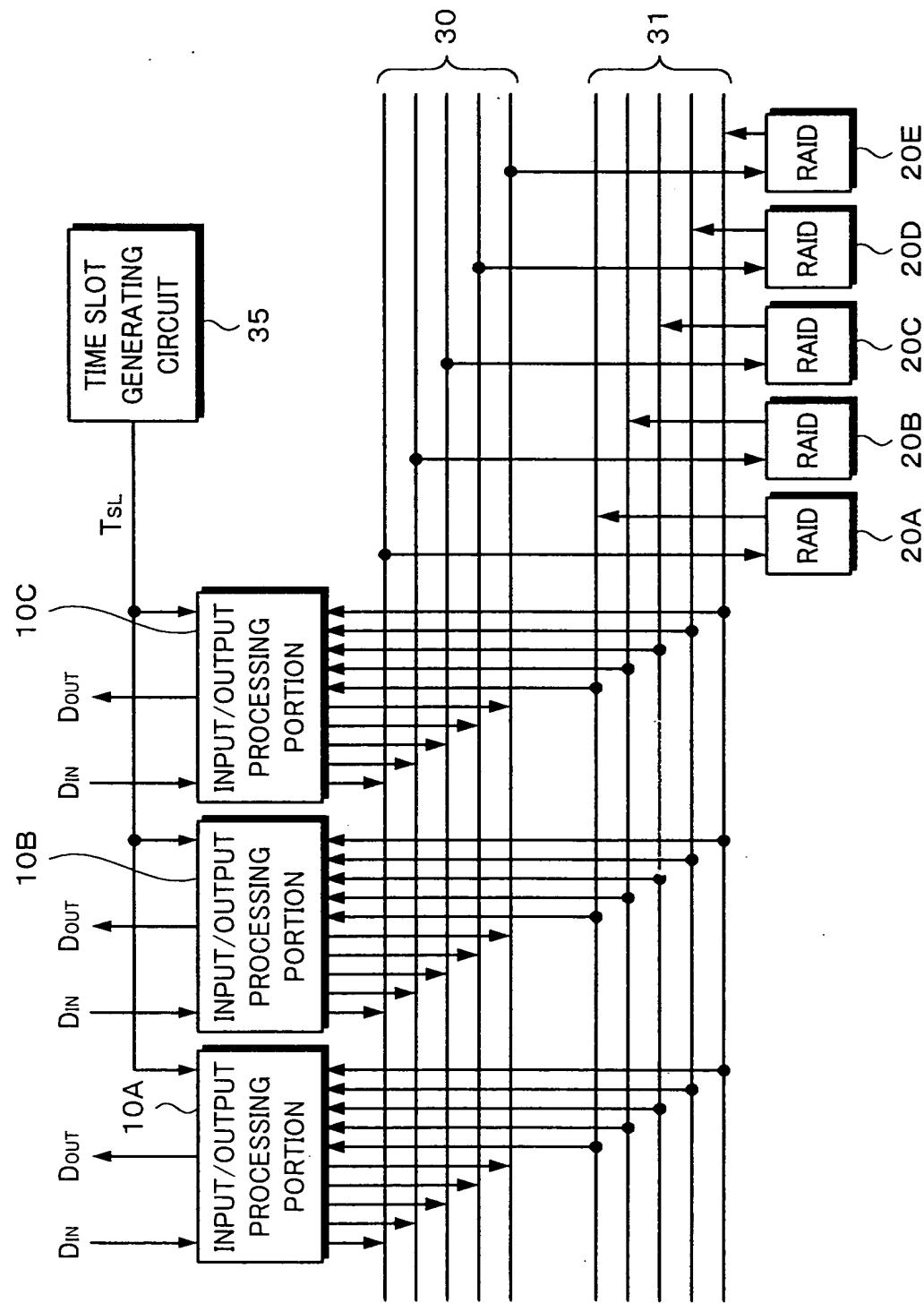


Fig. 3



TIME SLOT T_{SL}

12

(RECORDING SYSTEM)

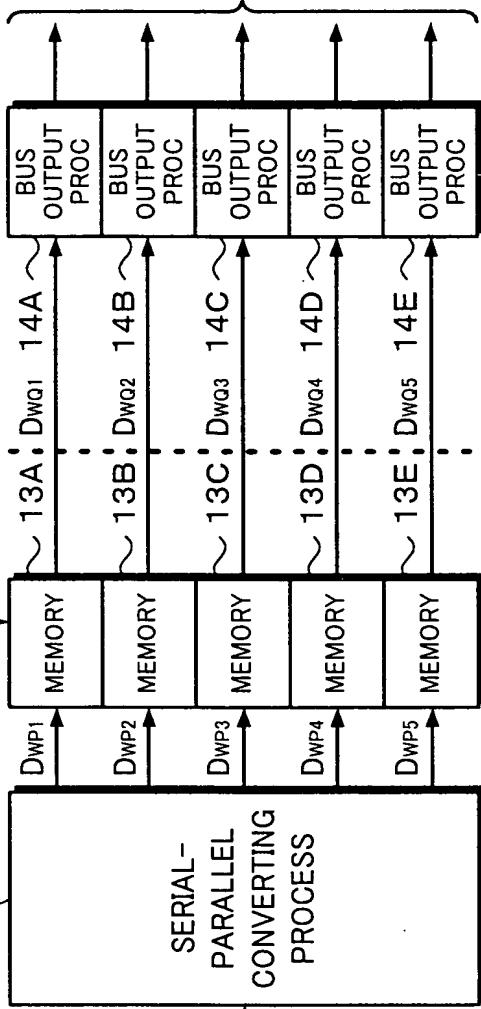
Fig. 4A

11

INPUT CIRCUIT

D_{IN}

SERIAL-
PARALLEL
CONVERTING
PROCESS



17

(REPRODUCING SYSTEM)

Fig. 4B

18

OUTPUT CIRCUIT

D_{OUT}

PARALLEL-
SERIAL
CONVERTING
PROCESS

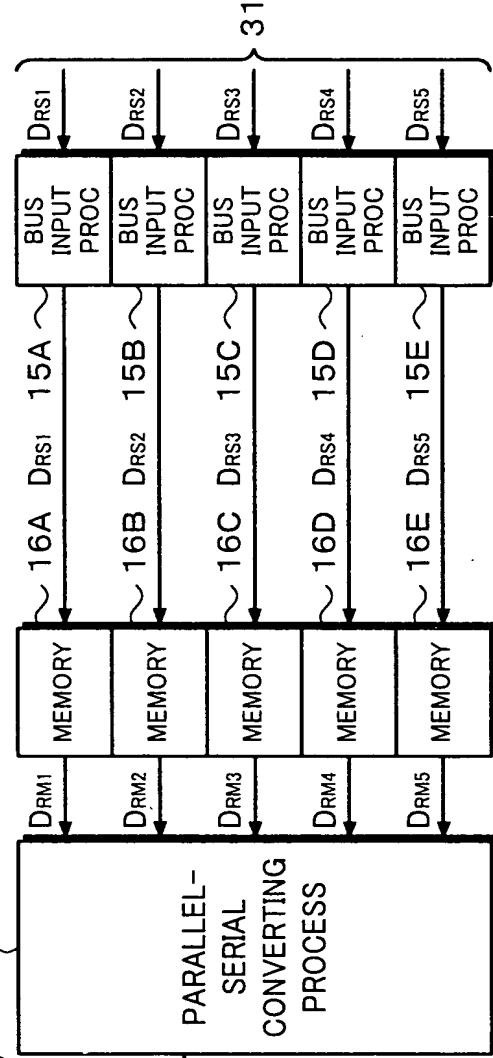


Fig. 5

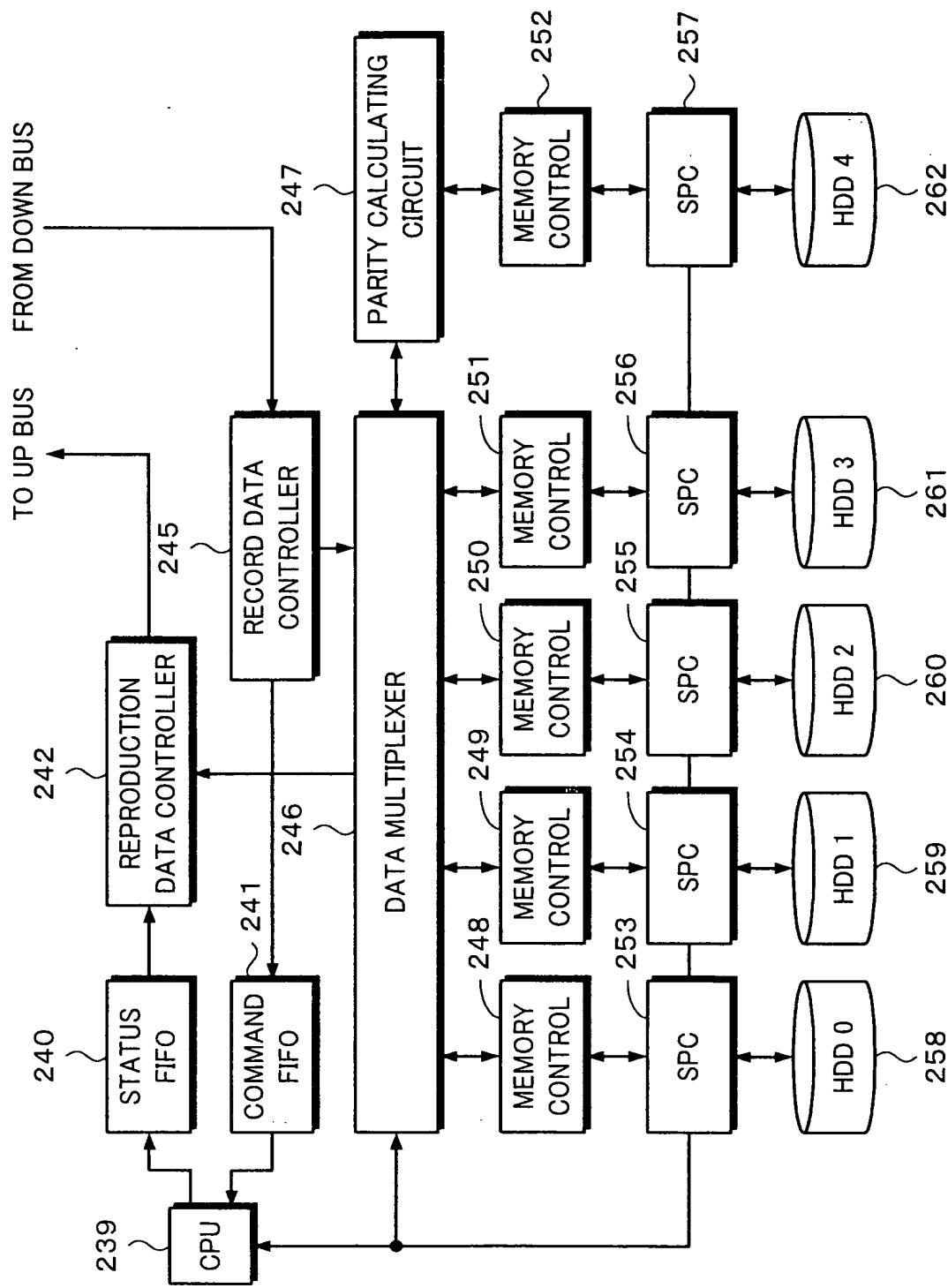


Fig. 6

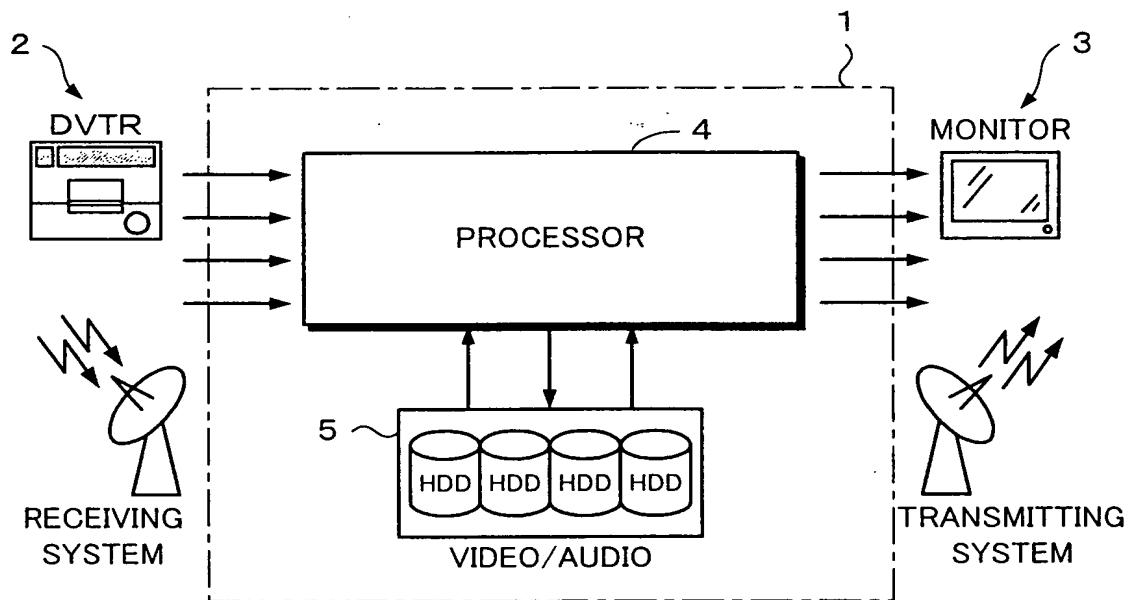


Fig. 7

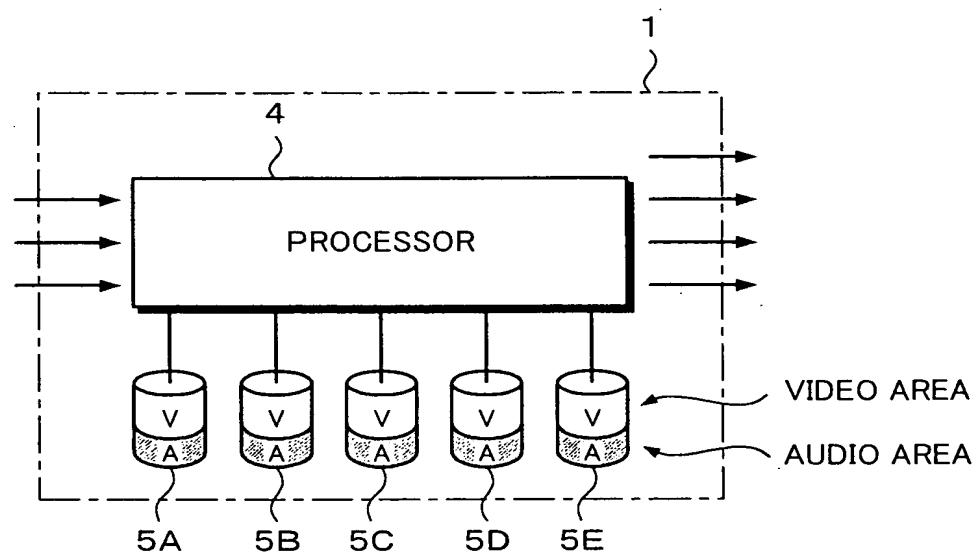


Fig. 8

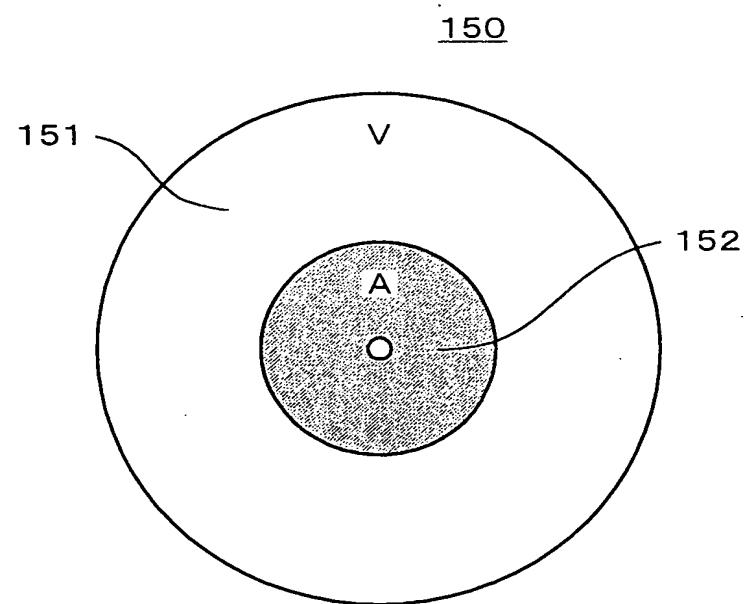


Fig. 9

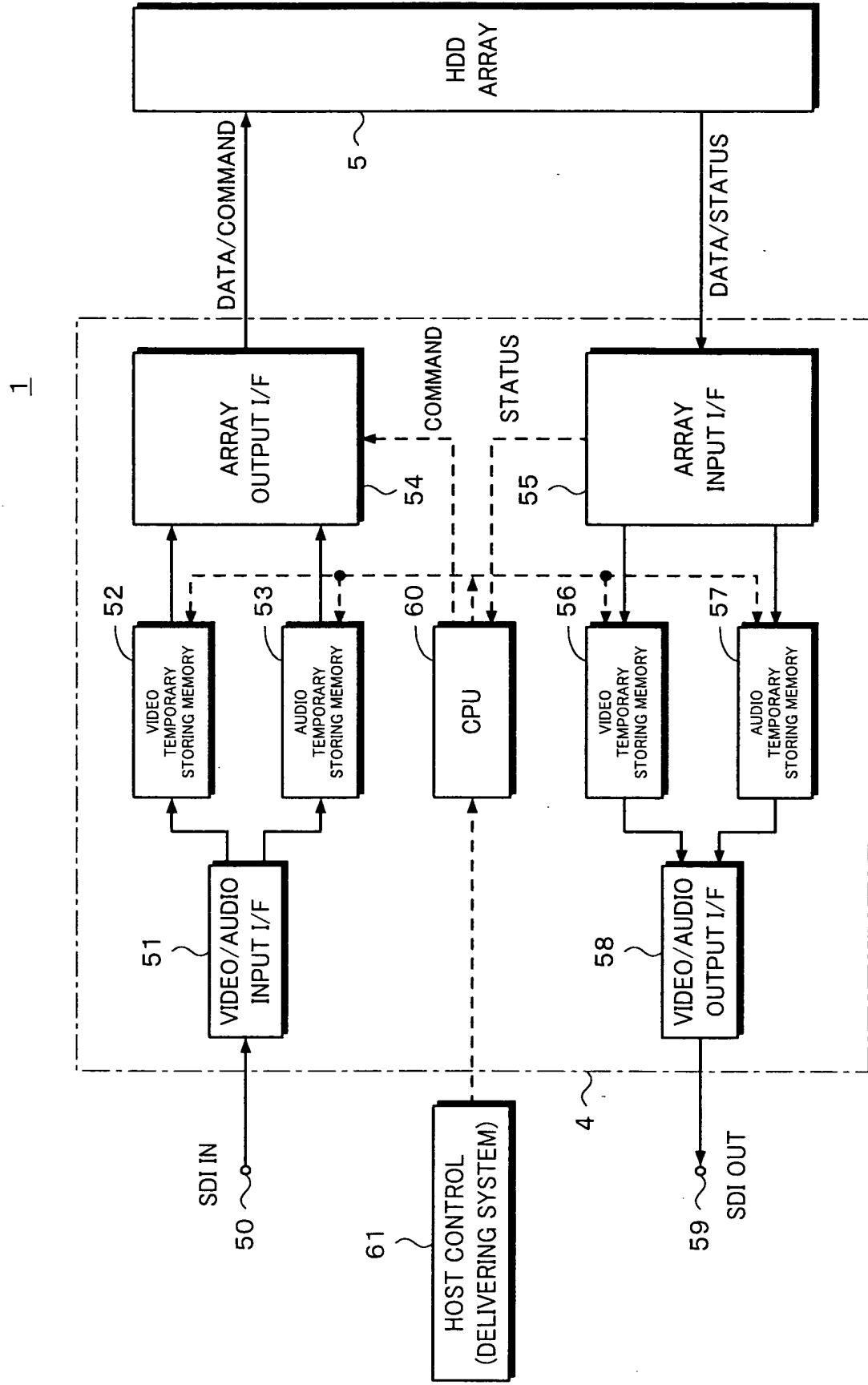


Fig. 10A

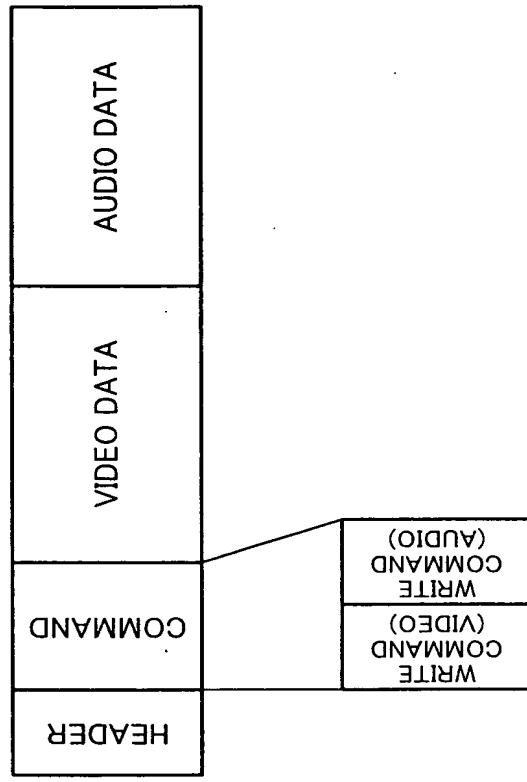


Fig. 10B

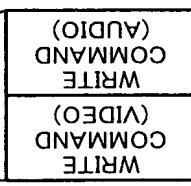


Fig. 10C

WRITE COMMAND (AUDIO) : FROM #00000001 TO #0001000
WRITE COMMAND (VIDEO) : FROM #10000001 TO #1001000

Fig. 11

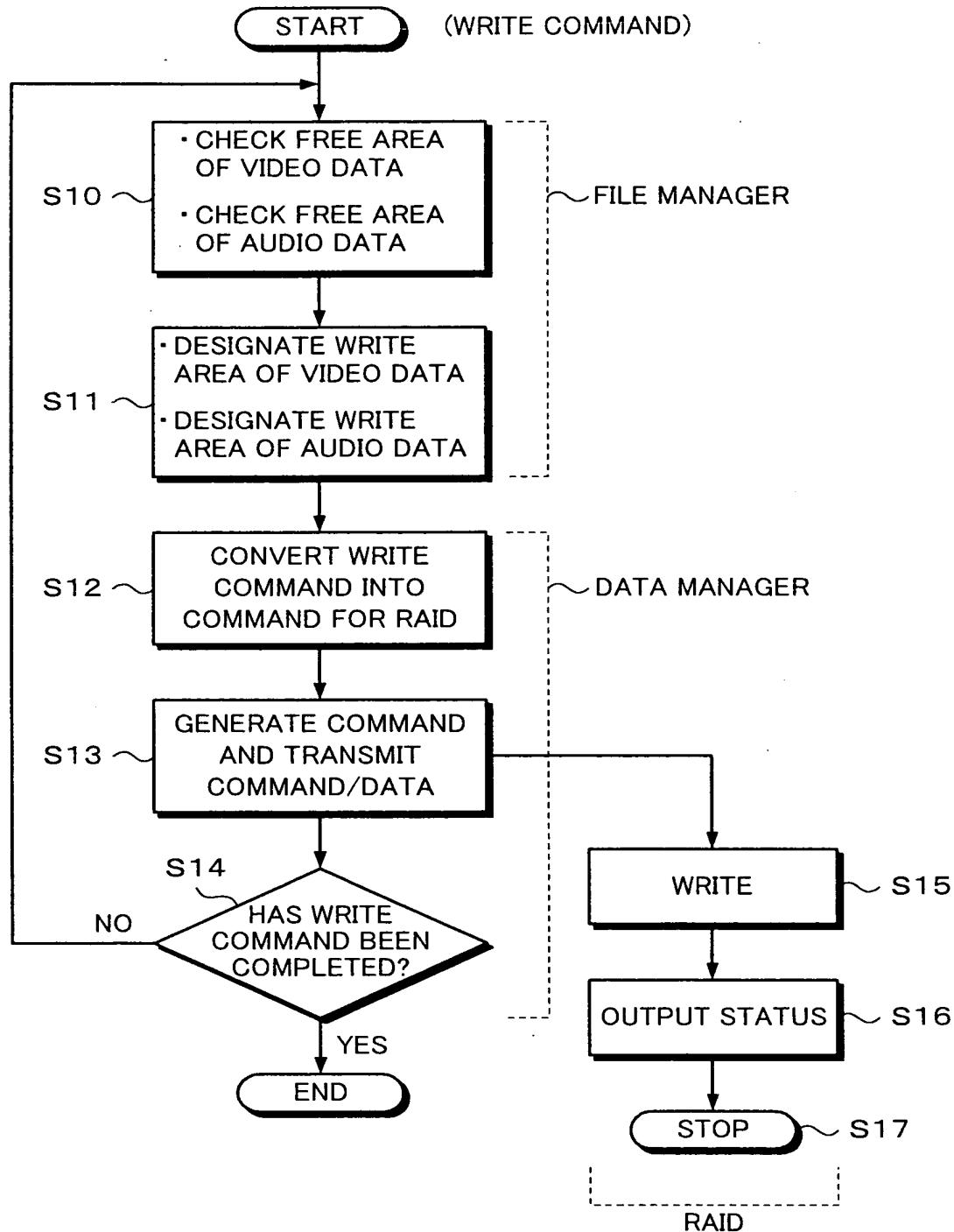


Fig. 12A

#0000001								
1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0
0	0			·	·	·	·	·

Fig. 12B

#1000001

Fig. 13

VIDEO DATA	16bit 4ch RAID-0	16bit 4ch RAID-1	20bit 4ch RAID-0	20bit 4ch RAID-1
AUDIO DATA				
20Mbps	75 : 25	62.5 : 37.5	72 : 28	57 : 43
30Mbps	83 : 17	71 : 29	80 : 20	67 : 33
40Mbps	86 : 14	76 : 24	84 : 16	72 : 28
50Mbps	89 : 11	80 : 20	86 : 14	76 : 24

Fig. 14A

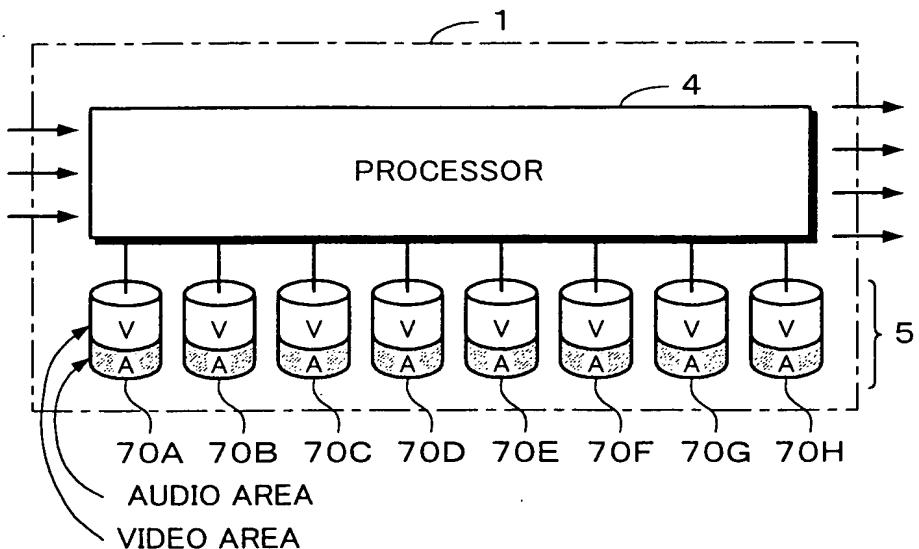


Fig. 14B

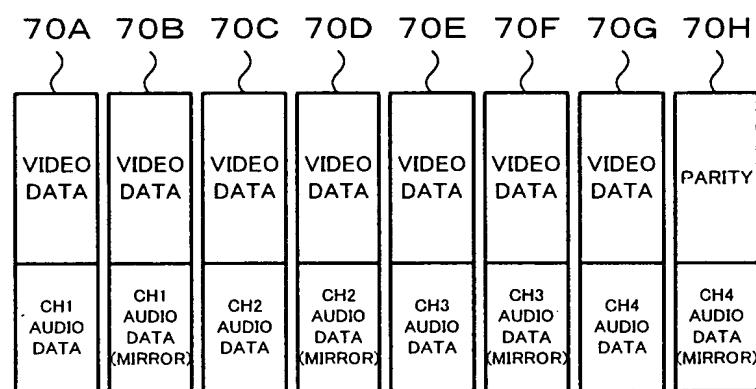


Fig. 14C

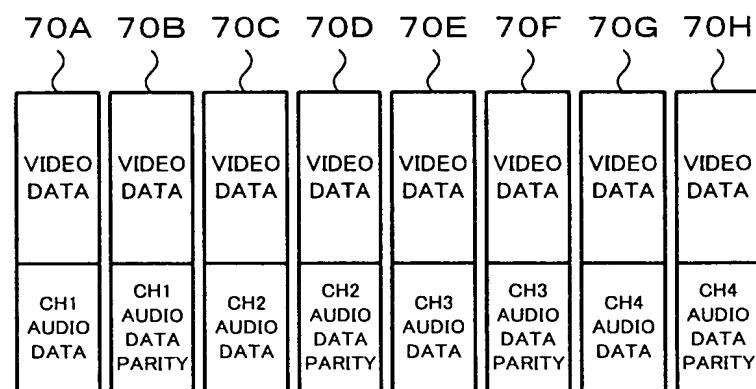


Fig. 14D

